FIG. 1(a)

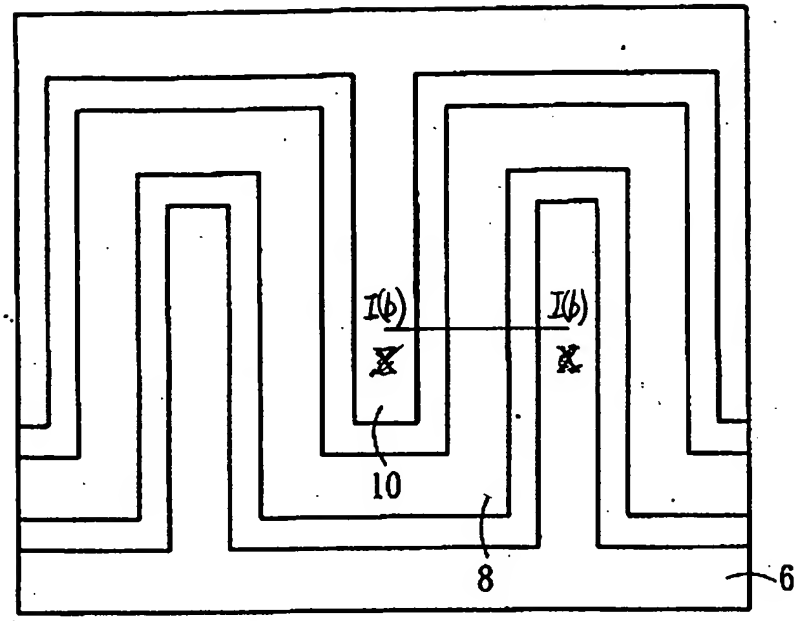
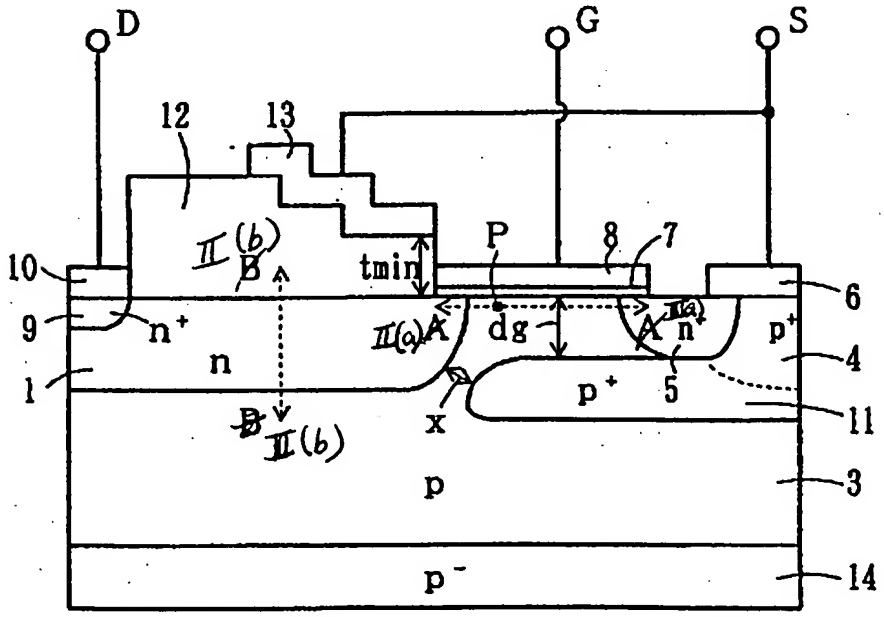


FIG. 1(b)



1: n-type drift region
2: p-type partition region
3: p-type base region
4: p^+-type contact region
5: n^+-type source region
6: Source electrode
7: Gate insulation film
8: Gate electrode
9: n^+-type drain region
10: Drain electrode
11: p^+-type stopper region
12: Oxide film
13: Field plate
14: p^--type substrate

FIG. 2(a)

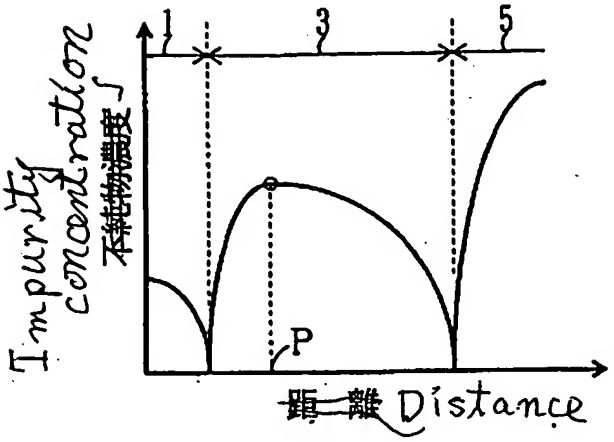


FIG. 2(b)

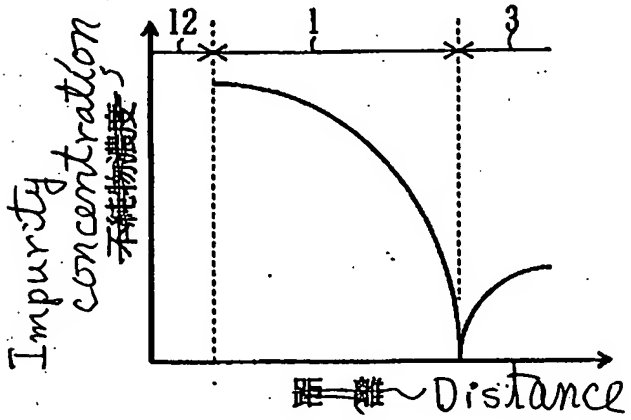
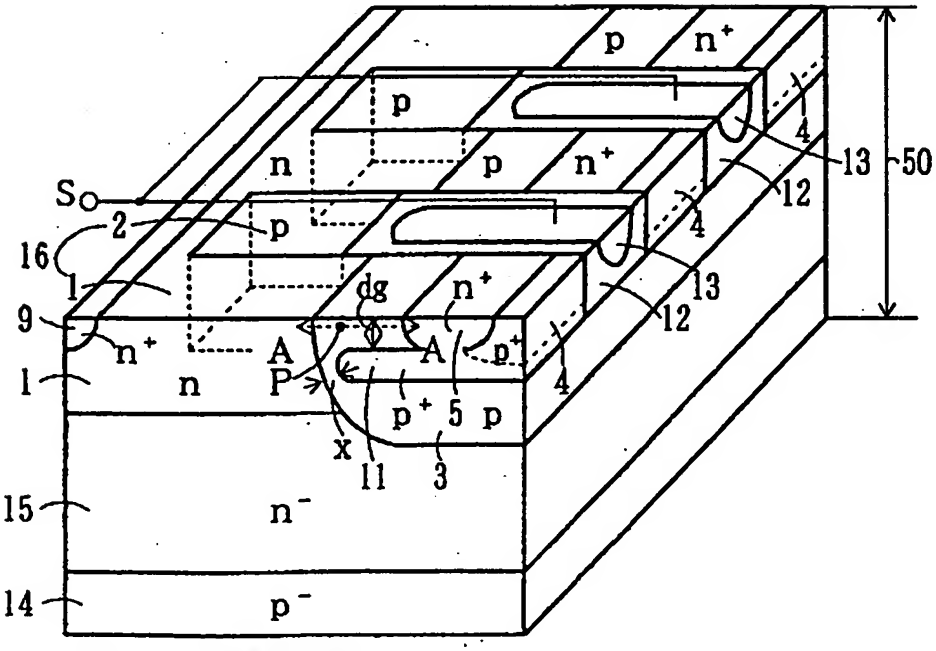


FIG. 3



50・・・半導体基板
Semiconductor substrate

FIG. 4

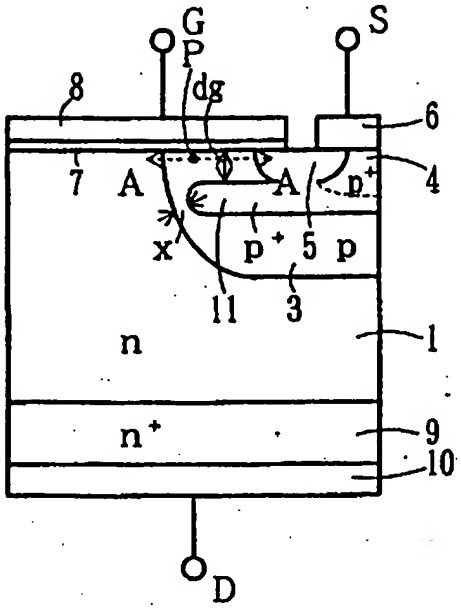

G
P
S
dg
8
6
7
A
A
p+
4
x
p+ 5 p
11
3
n
1
n+
9
10
D

FIG. 5

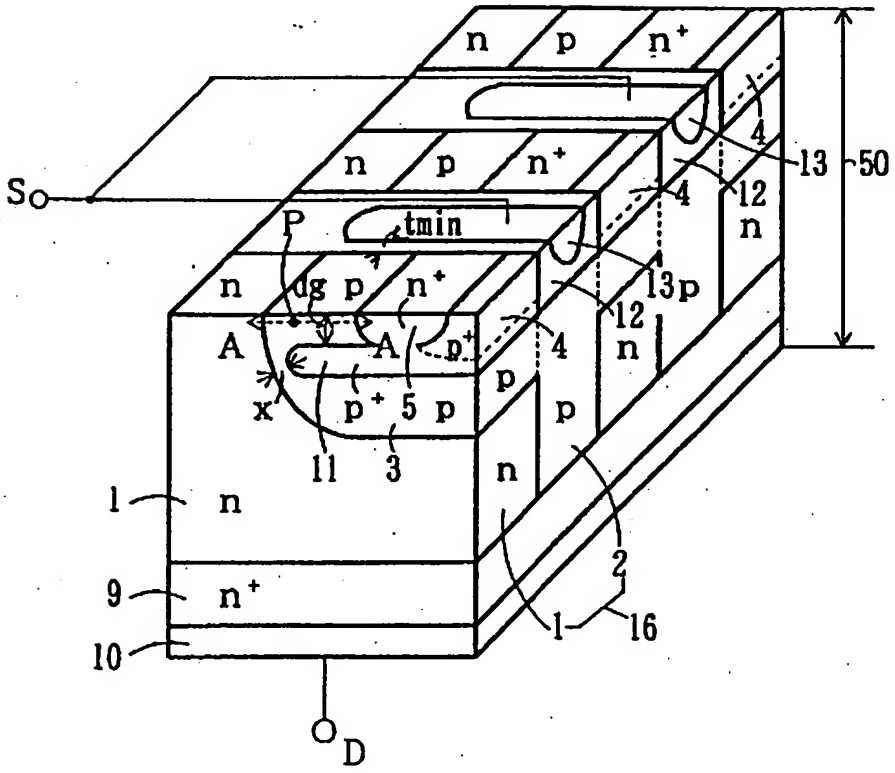

n p n+
4
13
50
So
n p n+
4
12
n
P
tmin
n dg p n+
13p
12
A
A
p+
4
n
x
p+ 5 p
p
p
11
3
n
1
n
2
9
n+
1
16
10
D

FIG. 6

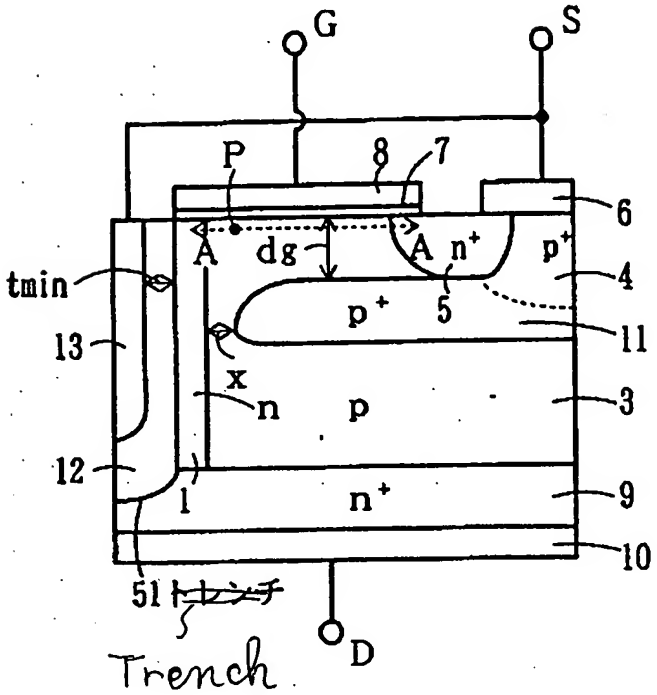

G
S
P
8
7
6
A
dg
A
n+
p+
tmin
4
p+
5
11
13
x
n
p
3
12
l
n+
9
10
51
D
Trench

FIG. 7

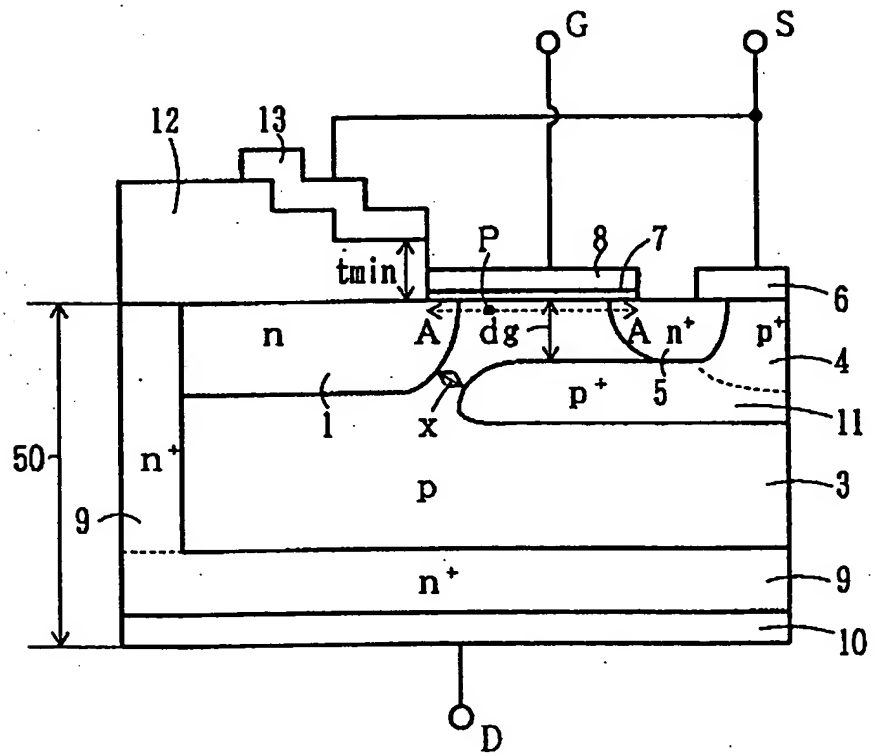
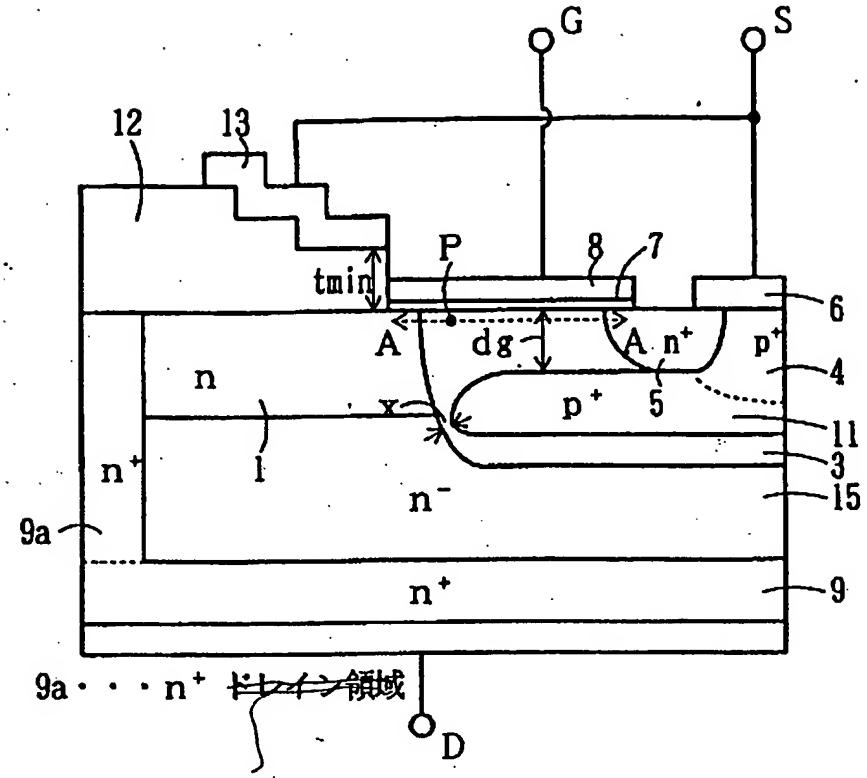

G
S
12
13
tmin
P
8
7
6
n
A
dg
A
n+
p+
4
p+
5
l
x
11
50
n+
p
3
9
n+
9
10
D

FIG. 8



Drain region

FIG. 9

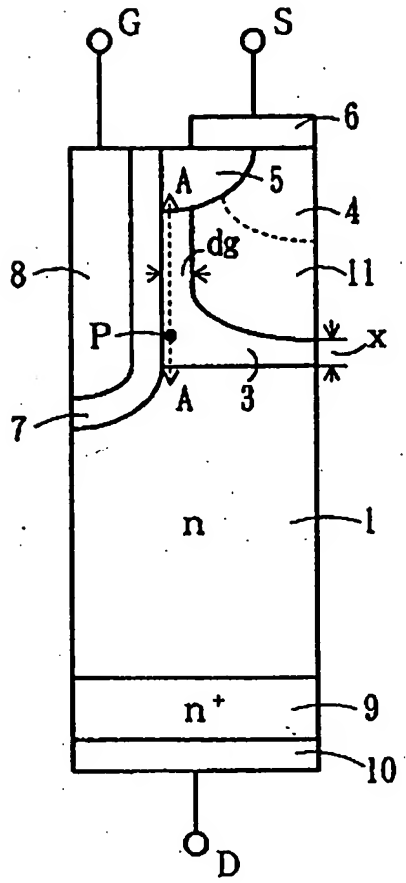


FIG. 10

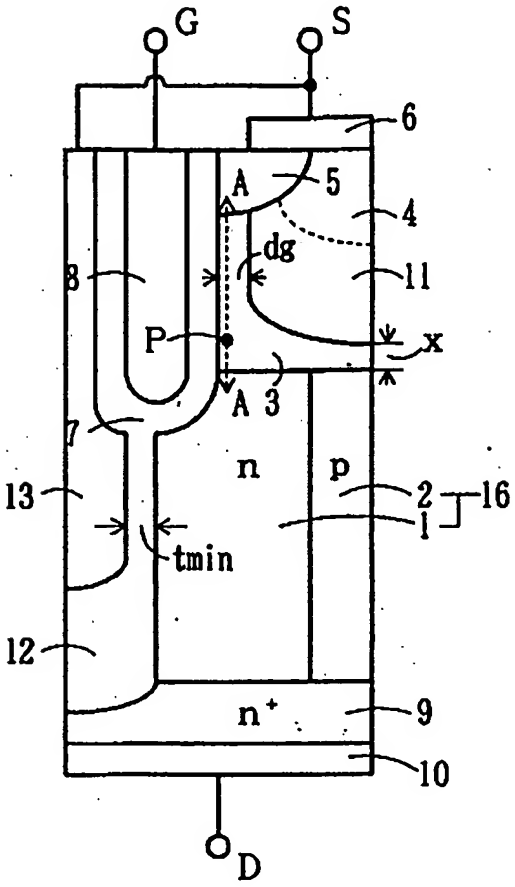


FIG. 11

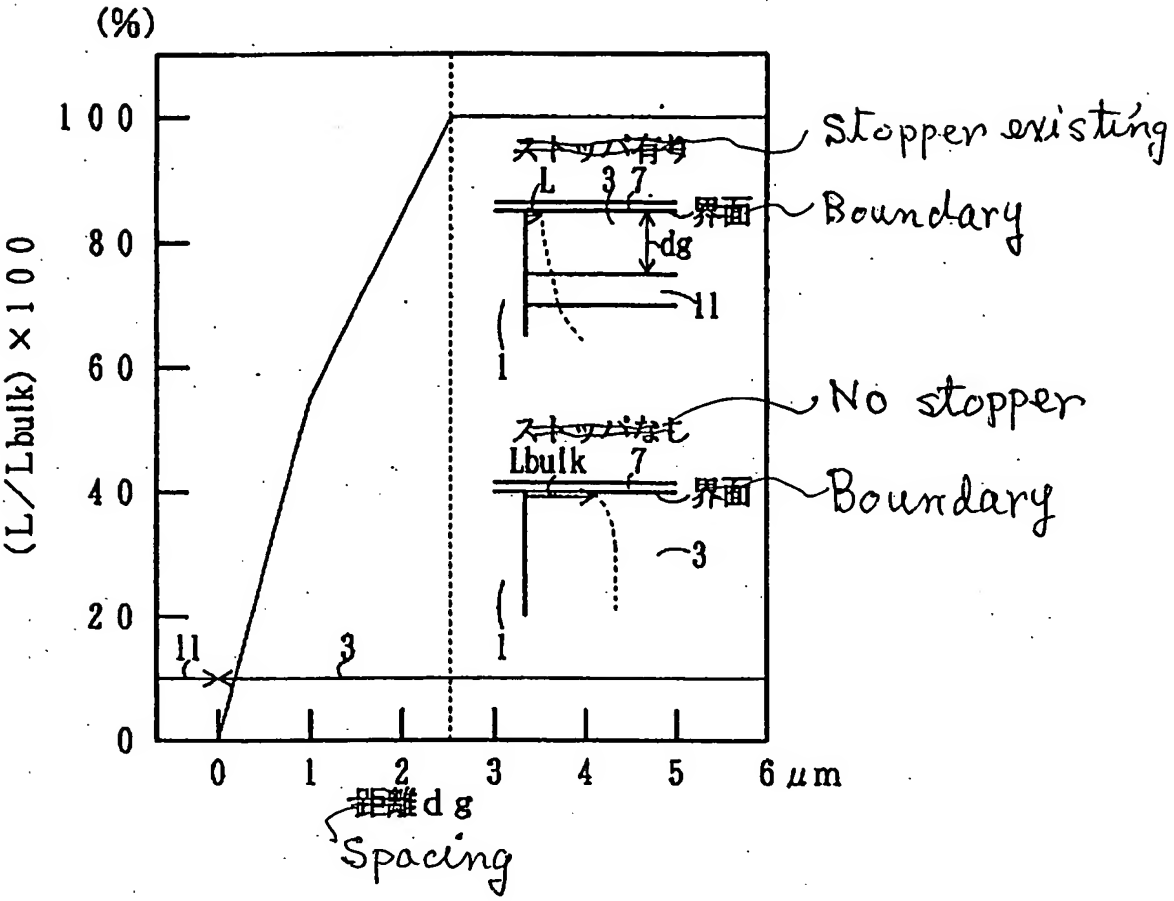

(%)
100
80
60
40
20
0
(L/Lbulk) ×100
0 1 2 3 4 5 6 μm
距離dg
Spacing
Stopper existing
ストッパ有り
L 37
界面
Boundary
dg
11
1
No stopper
ストッパなし
Lbulk 7
界面
Boundary
3
11
3
1

FIG. 12

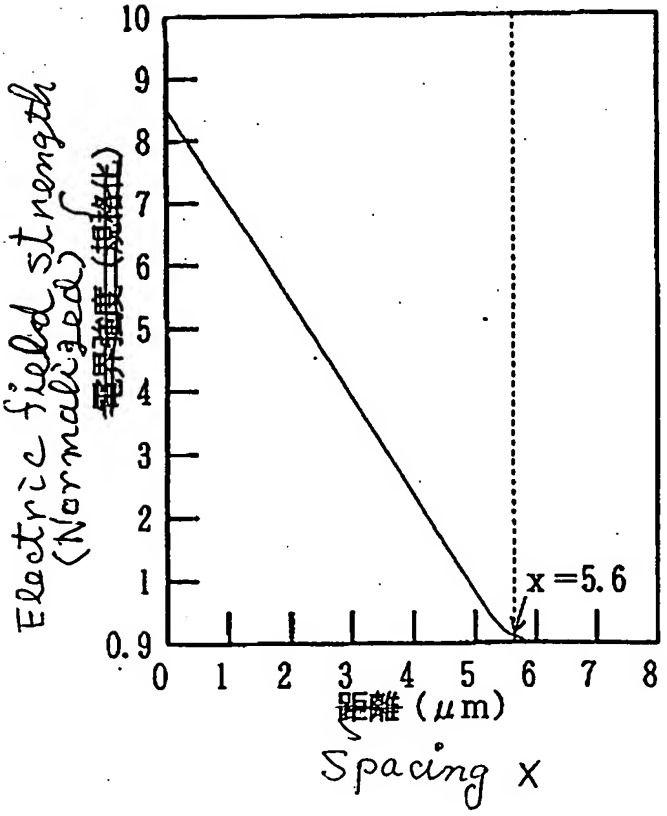
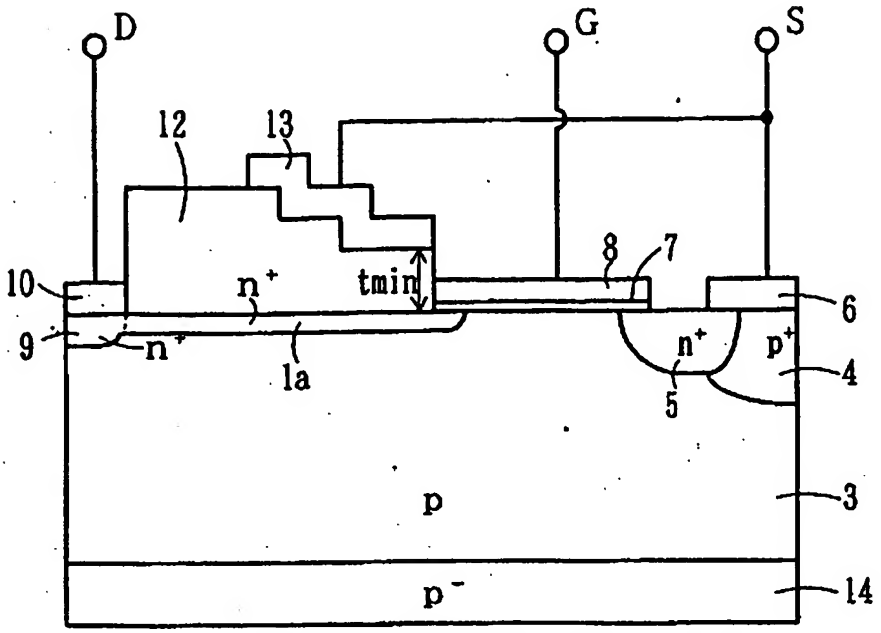
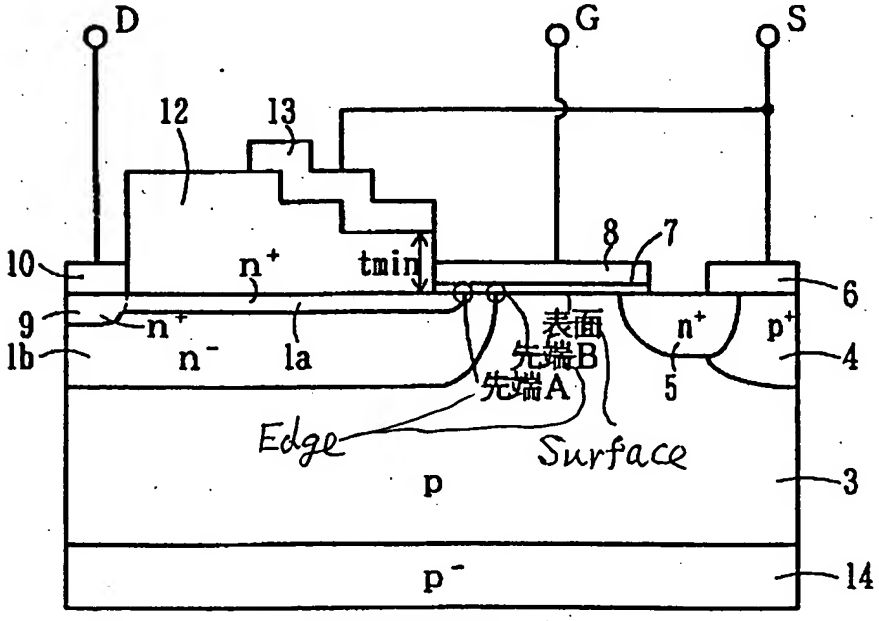

Electric field strength
(Normalized)
電界強度(規格化)
10
9
8
7
6
5
4
3
2
1
0.9
0 1 2 3 4 5 6 7 8
x=5.6
距離(μm)
Spacing x

FIG. 13



la・・・n+ ~~ドリフト領域~~ drift region

FIG. 14



lb・・・n- ~~ドリフト領域~~

drift region

FIG. 15

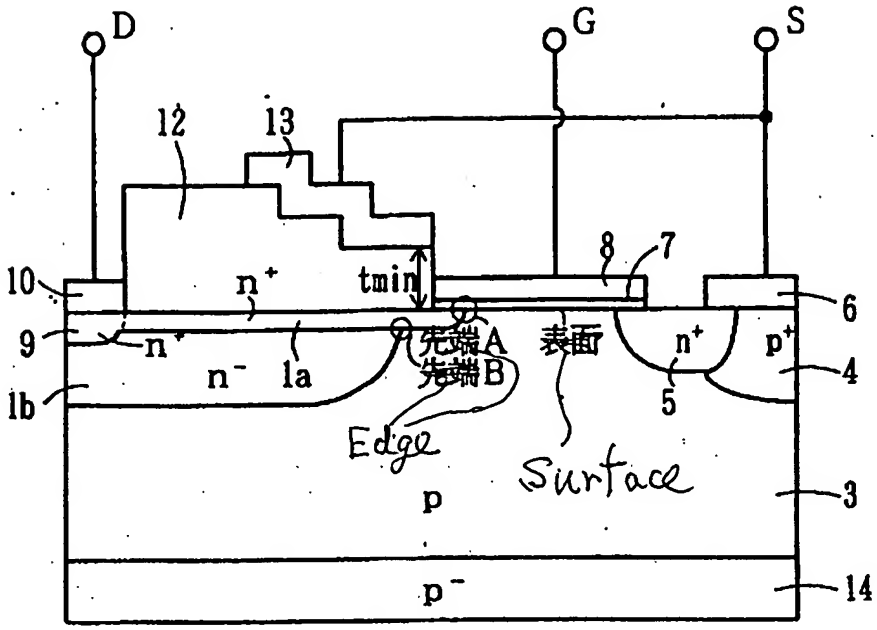

D
G
S
12
13
8
7
10
n+
tmin
6
9
n+
先端A
表面
n+
p+
n-
1a
先端B
4
1b
5
Edge
Surface
p
3
p-
14

FIG. 16

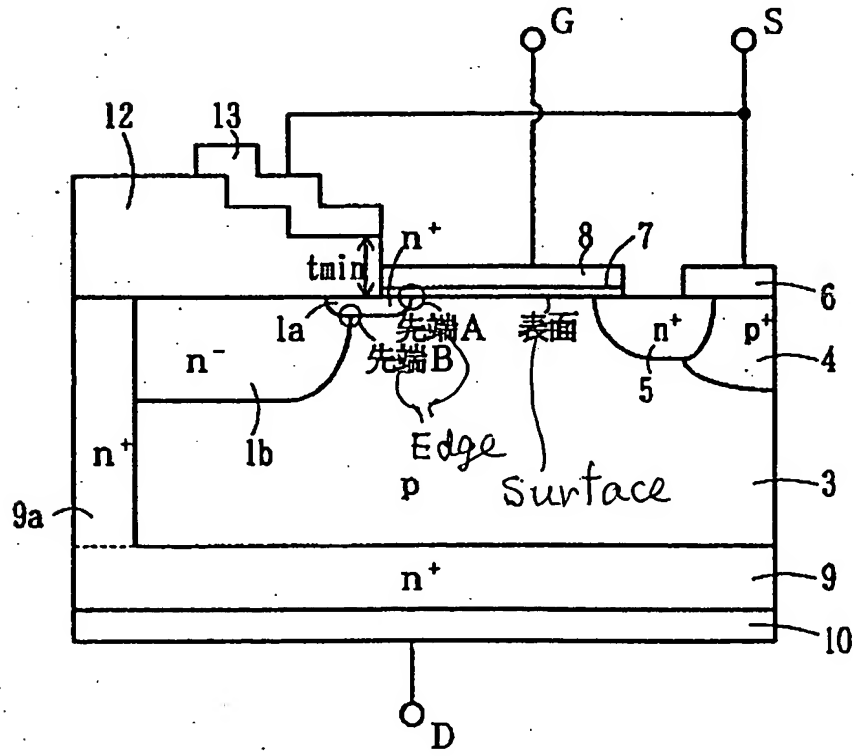
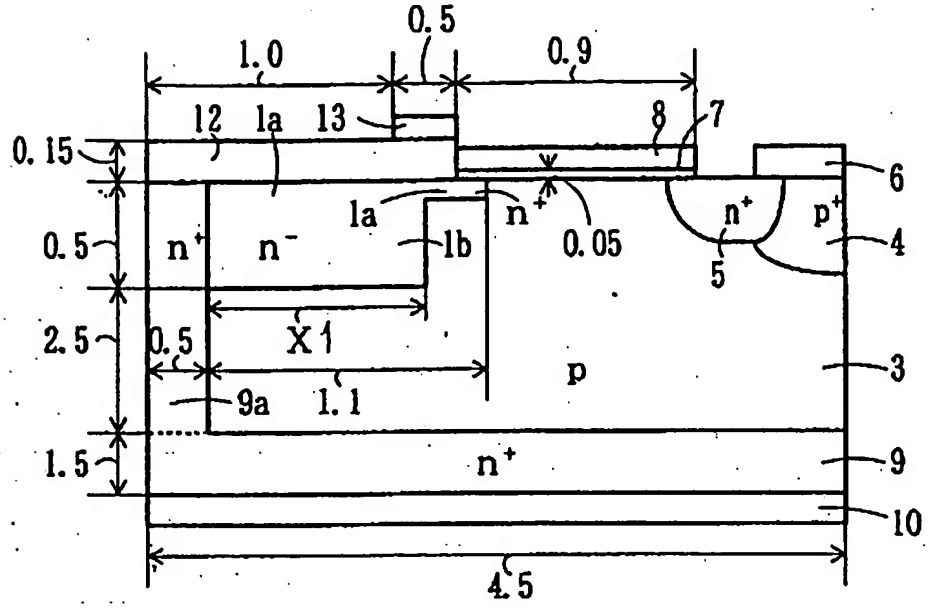

G
S
12
13
n+
8
7
tmin
6
1a
先端A
表面
n+
p+
n-
先端B
4
5
n+
1b
Edge
p
Surface
3
9a
n+
9
10
D

FIG. 17



Unit of the Numerals: μ m

Impurity Concentrations and Impurity Atoms

Heavily doped drift region 1a (n^+)	:	3×10^{17} cm^{-3} (As)
Lightly doped drift region 1b (n^-)	:	6×10^{16} cm^{-3} (P)
p-type base region 3	:	1.5×10^{16} cm^{-3} (B)
n^+-type drain region 9	:	1.2×10^{19} cm^{-3} (As)
n^+-type drain region 9a	:	1.2×10^{19} cm^{-3} (P)

FIG. 18

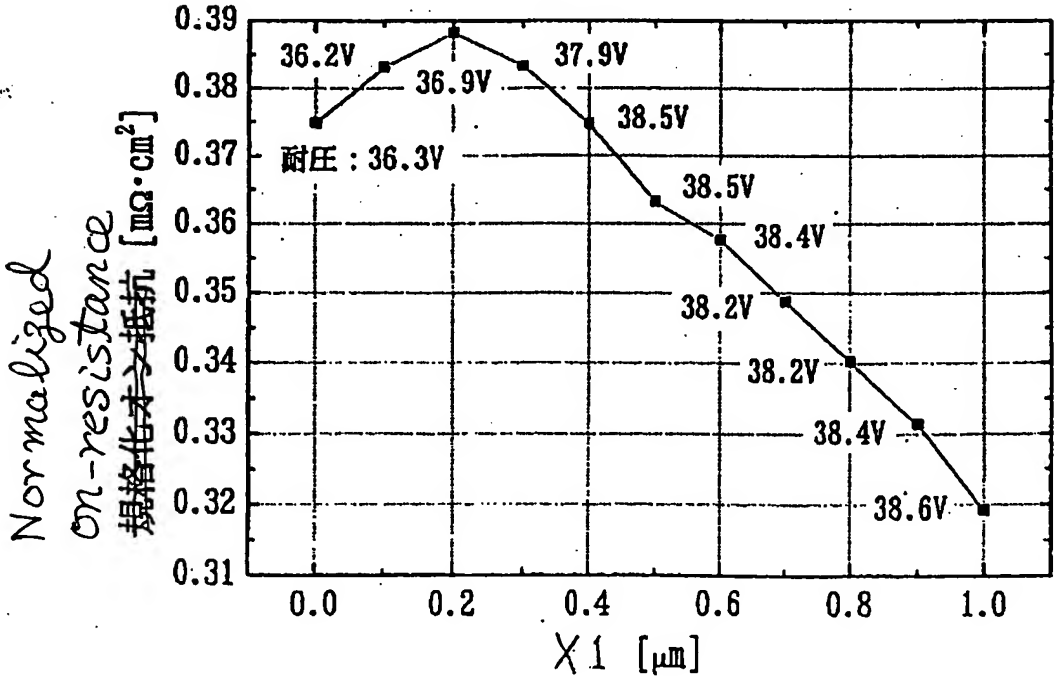


FIG. 19

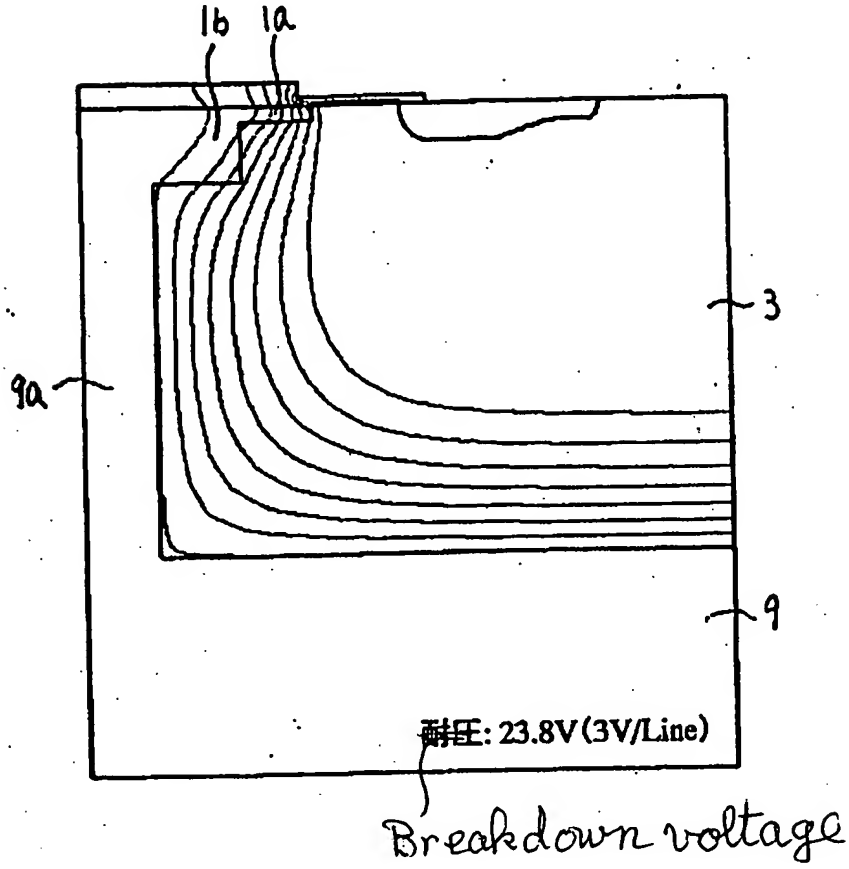


FIG. 20

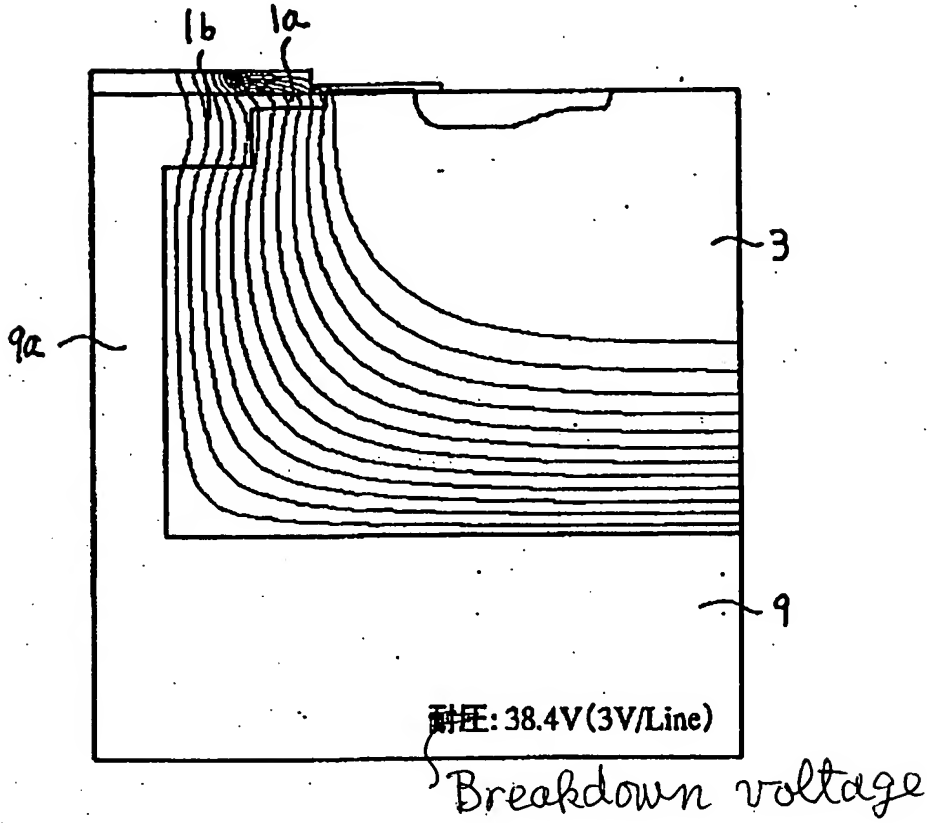

1b
1a
3
9a
9
耐圧: 38.4V(3V/Line)
Breakdown voltage

FIG. 21

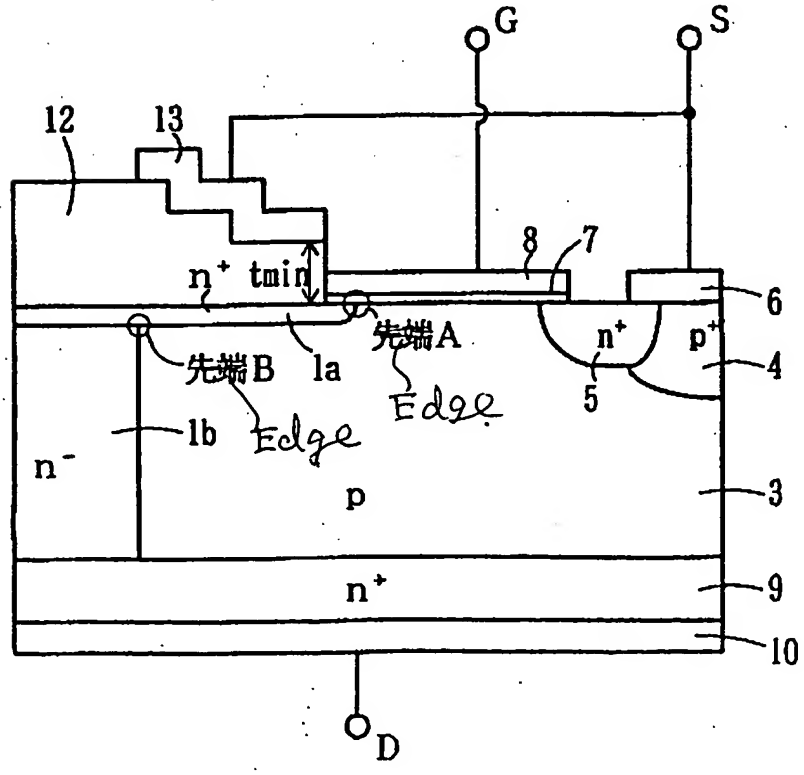

G
S
12
13
8
7
n+ tmin
6
先端B
1a
先端A
n+
p+
4
Edge
Edge
5
1b
n-
p
3
n+
9
10
D

FIG. 22

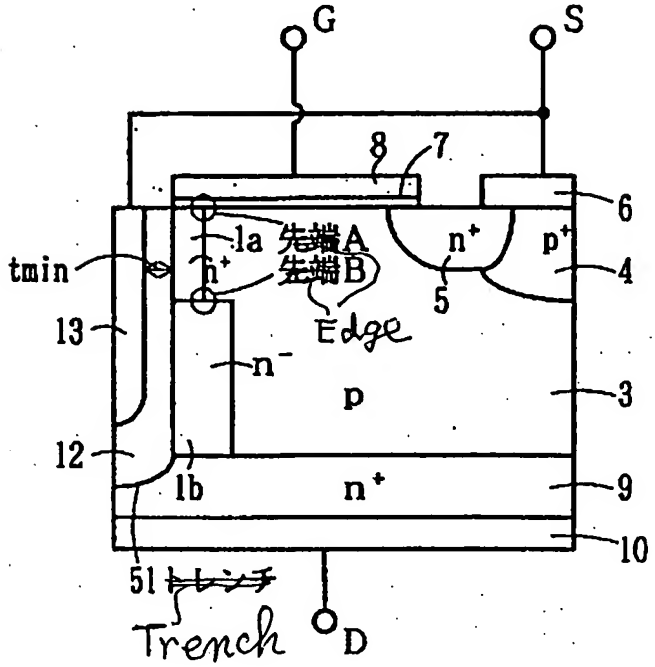

G
S
8
7
6
1a
先端A
n+
p+
tmin
h+
先端B
4
5
13
Edge
n-
p
3
12
1b
n+
9
10
51
Trench
D

FIG. 23

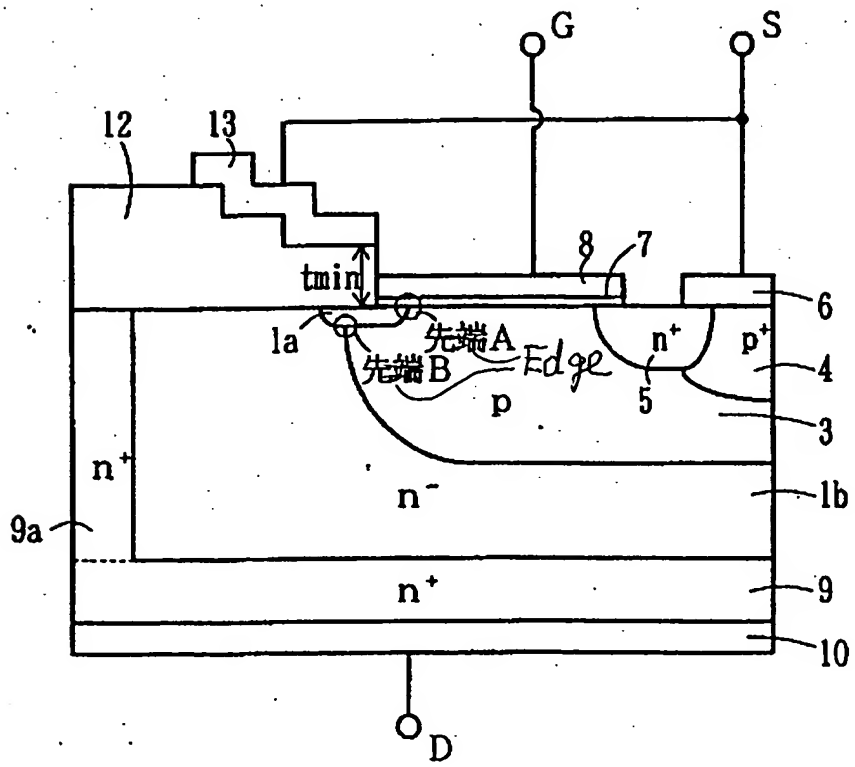

G
S
12
13
8
7
tmin
6
1a
先端A
n+
p+
先端B
Edge
4
p
5
3
n+
n-
1b
9a
n+
9
10
D

FIG. 24

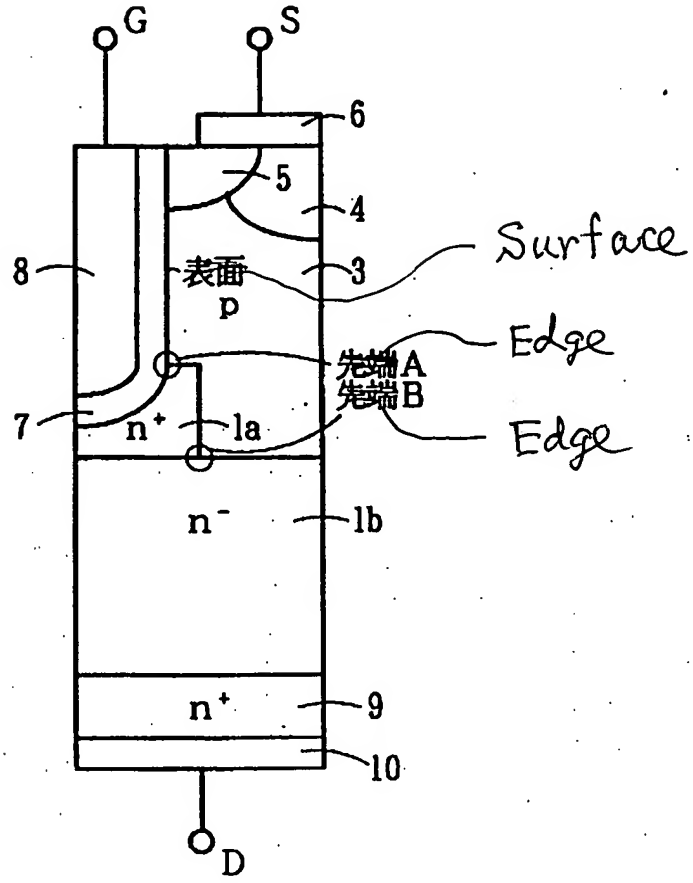
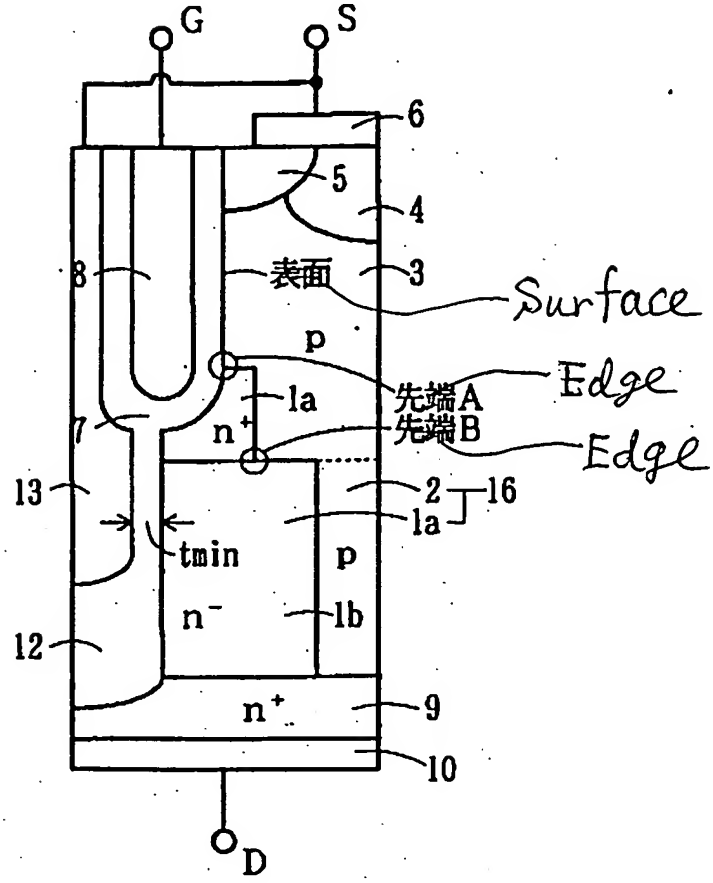


FIG. 25



【図２６】

FIG. 26

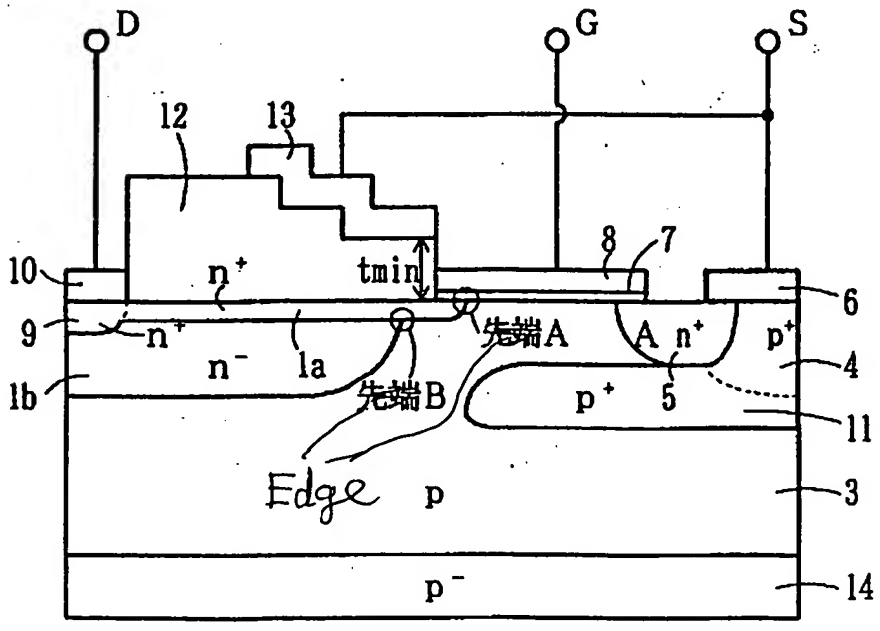
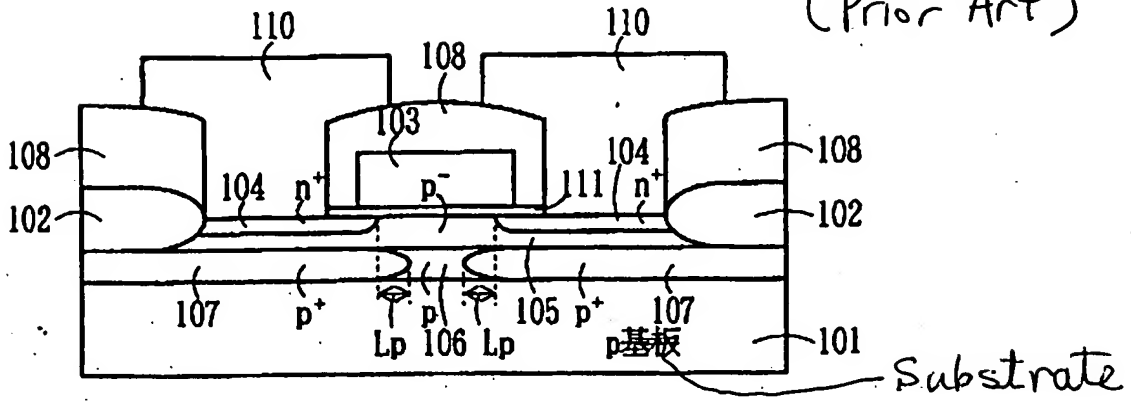
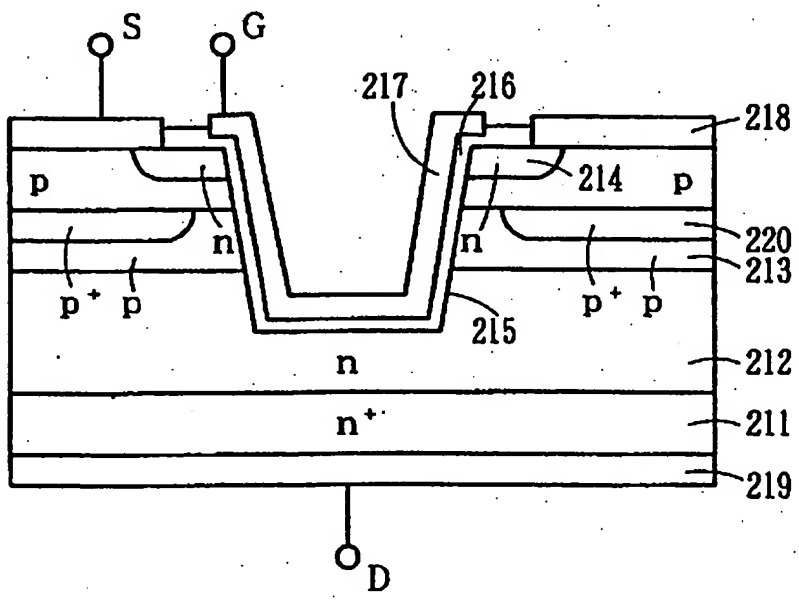


FIG. 27
(Prior Art)



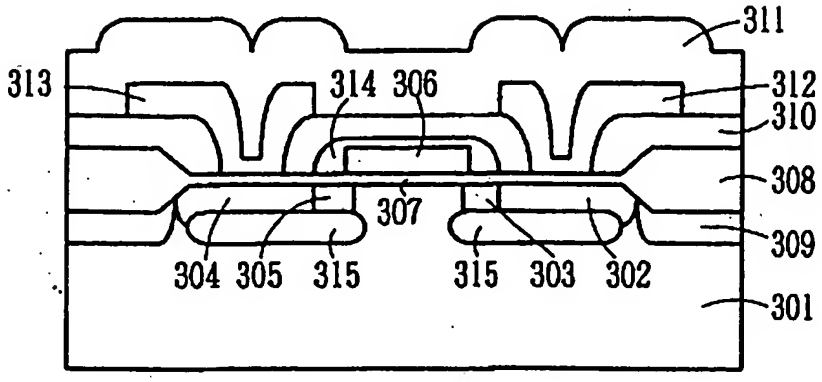
101:	Silicon substrate	106:	Heavily doped buried region
102:	Device separation film	107	Heavily doped buried region
103	Gate electrode	108:	Interlayer insulation film
104:	Source/Drain	110:	Aluminum wiring layer
105:	Lightly doped surface layer	111:	Gate insulation film

FIG. 28
(Prior Art)



211:	n^+-type substrate	216:	Gate oxide film
212:	n-type drift layer	217	Gate electrode
213	p-type base layer	218:	Source electrode
214:	n-type source layer	219:	Drain electrode
215:	Trench	220:	p^+-type buried region

FIG. 29
(Prior Art)



301:	Well region	308:	Field oxide film
302:	Heavily doped drain region	309	Field doped region
303	Lightly doped drain region	310:	Interlayer insulation film
304:	Heavily doped source region	311:	Protection film
305:	Lightly doped source region	312:	Drain wiring
306:	Gate electrode	313:	Source wiring
307:	Gate oxide film	315:	Impurity region